







User Experiments with PGAS Languages, or







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Will Sawyer, Sergei Isakov, Adrian Tineo







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Use scientifically relevant mini-apps from communities to:

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Use *scientifically relevant* mini-apps from communities to:

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- Evaluate programming paradigms
 - MPI + OpenMP hybrid programming
 - MPI-2 one-sided communication
 - SHMEM
 - PGAS languages (CAF, UPC)
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 - SHMEM
 - PGAS languages (CAF, UPC)
 - OpenACC, CUDA, OpenCL, if possible
- Compare performance across platforms
 - out-of-the-box performance
 - evaluate optimization effort
 - socket-for-socket, node-for-node, energy-to-solution comparisons









PGAS: Partitioned Global Address Space





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- UPC: Unified Parallel C





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- SHMEM: Shared Memory API (SGI)







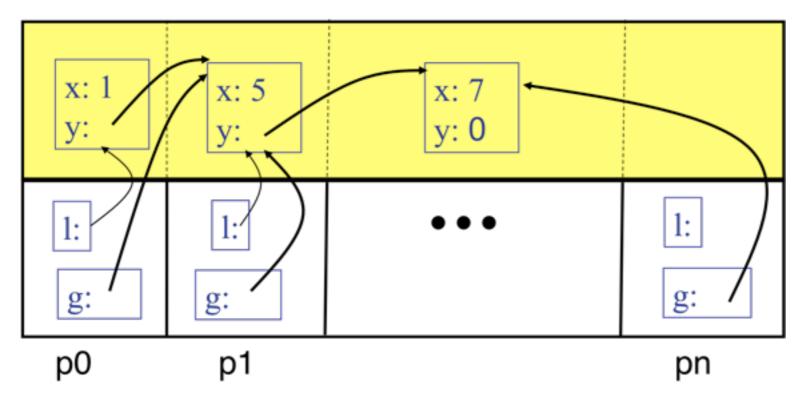


- Global address space: any thread/process may directly read/write data allocated by any other
- Partitioned: data is designated as local or global; programmer controls layout





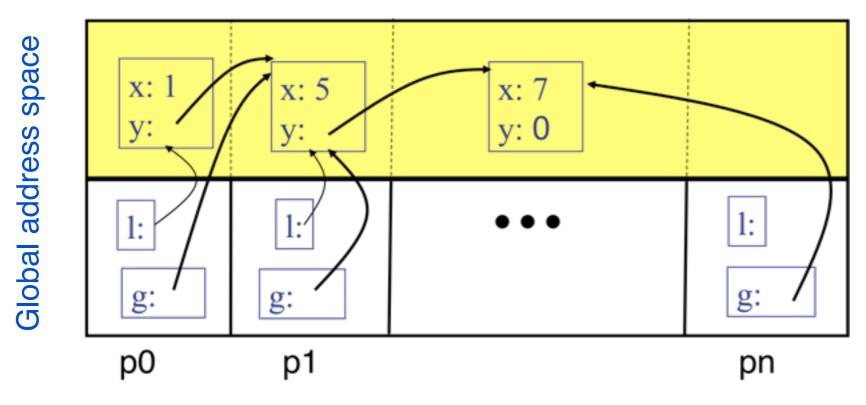
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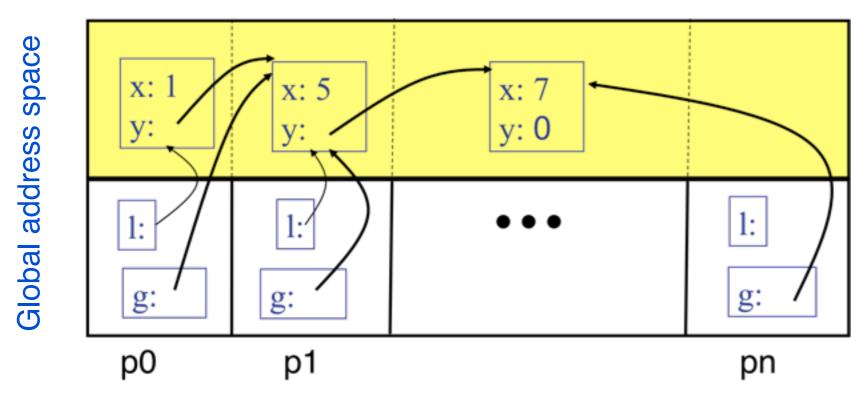
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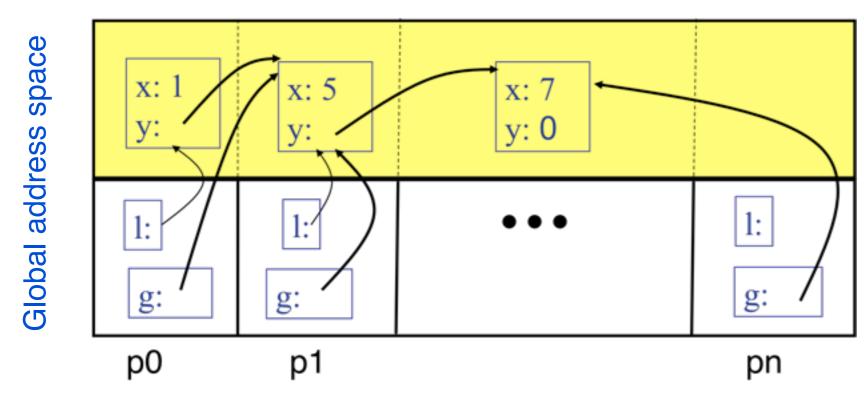
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3 Current languages: UPC, CAF, and Titanium





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PGAS hardware support available

- Cray Gemini (XE6) interconnect supports RDMA
- Potential interoperability with existing C/Fortran/Java code

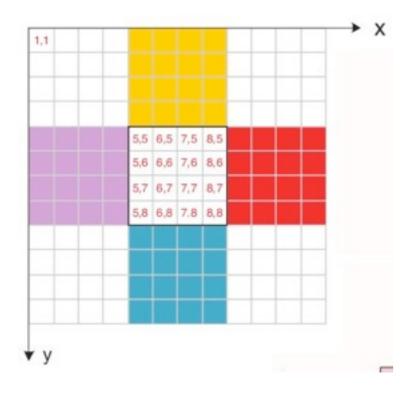


Problem 1: Halo Exchange

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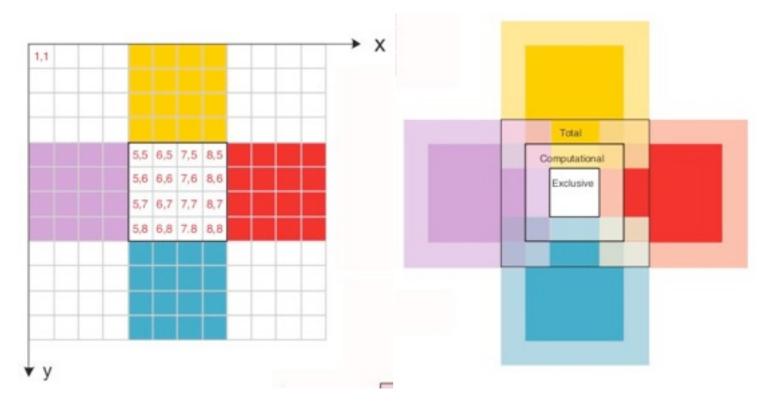


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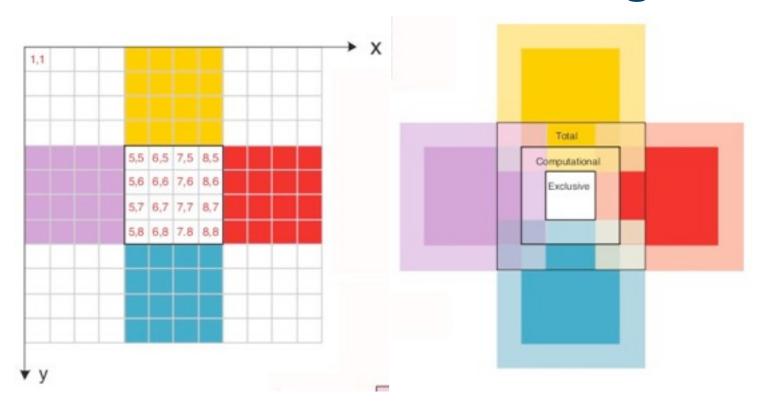


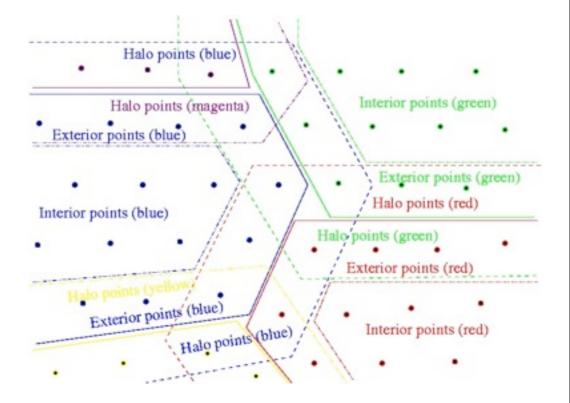
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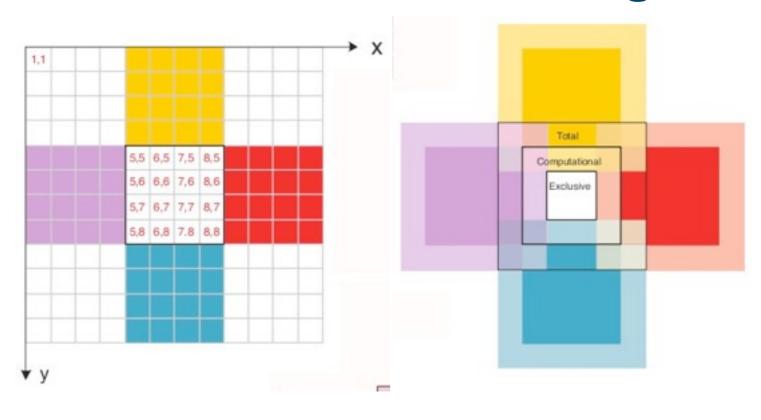
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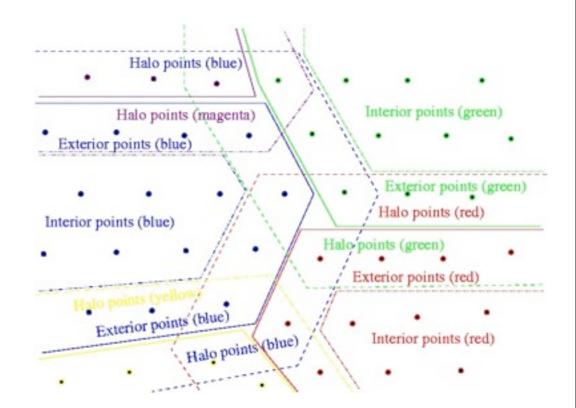


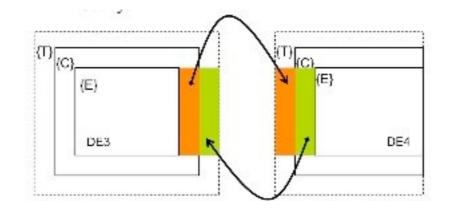




Problem 1: Halo Exchange











Potential Performance Gains with Co-Array Fortran

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Potential Performance Gains with Co-Array Fortran

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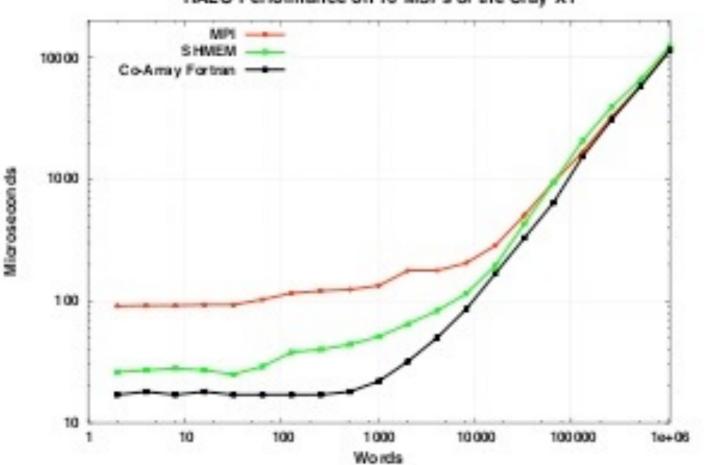


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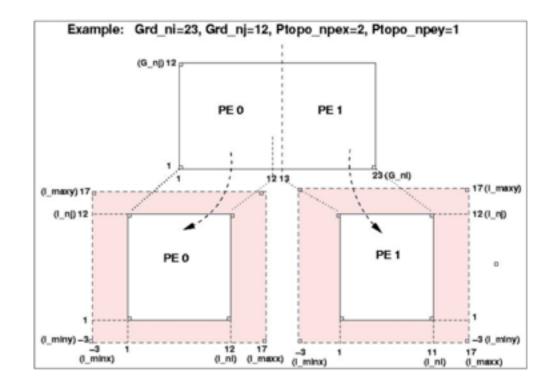
HALO Performance on 16 MSPs of the Cray X1

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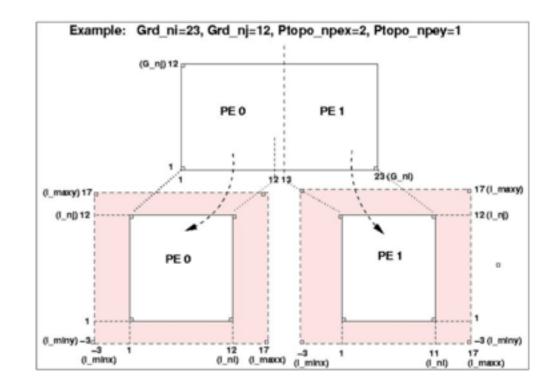
Halo Exchange "Stencil 2D" Benchmark







Halo exchange and stencil operation over a square domain distributed over a 2-D virtual process topology

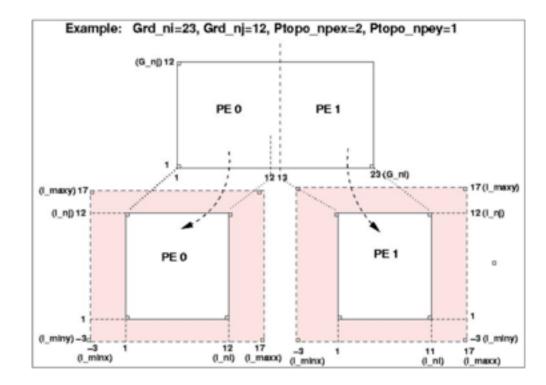






Halo exchange and stencil operation over a square domain distributed over a 2-D virtual process topology

• Arbitrary halo 'radius' (number of halo cells in a given dimension, e.g. 3)

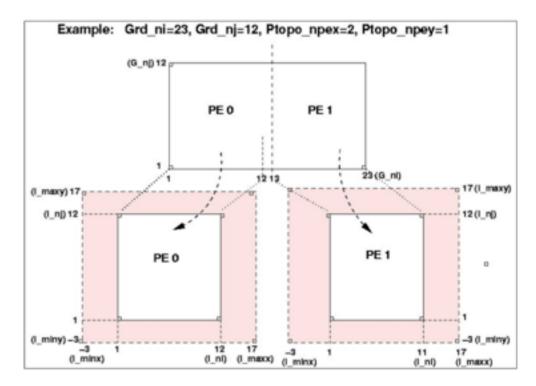






Halo exchange and stencil operation over a square domain distributed over a 2-D virtual process topology

- Arbitrary halo 'radius' (number of halo cells in a given dimension, e.g. 3)
- MPI implementations:
 - Trivial: post all 8 MPI_Isend and Irecv
 - Sendrecv: MPI_Sendrecv between PE pairs
 - Halo: MPI_Isend/Irecv between PE pairs

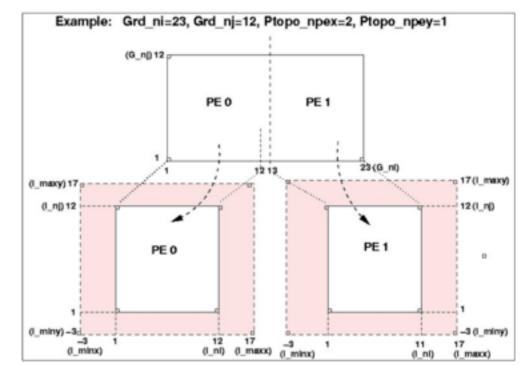






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- CAF implementations:
 - Trivial: simple copies to remote images
 - Put: reciprocal puts between image pairs
 - Get: reciprocal gets between image pairs
 - Get0: all images do inner region first, then all do block region (fine grain, no sync.)
 - Get1: half of images do inner region first, half do block region first (fine grain, no sync.)





Example code: Trivial CAF

```
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich
```



Example code: Trivial CAF

```
real, allocatable, save :: V(:,:)[:,:]
  :
 allocate( V(1-halo:m+halo,1-halo:n+halo)[p,*] )
  :
 WW = myP-1; if (WW < 1) WW = p
 EE = myP+1; if (EE>p) EE = 1
 SS = myQ-1; if (SS<1) SS = q
 NN = myQ+1; if (NN>q) NN = 1
    :
                                    = dom(1:m, 1:n)
 V(1:m,1:n)
                                                                   ! computational region
 V(1-halo:0, 1:n)[EE,myQ]
                                    = dom(m-halo+1:m, 1:n)
                                                                   1
                                                                     to East
 V(m+1:m+halo, 1:n)[WW,myQ]
                                    = dom(1:halo,1:n)
                                                                   ! to West
 V(1:m,1-halo:0)[myP,NN]
                                    = dom(1:m,n-halo+1:n)
                                                                   ! to North
 V(1:m,n+1:n+halo)[myP,SS]
                                    = dom(1:m, 1:halo)
                                                                   ! to South
 V(1-halo:0,1-halo:0)[EE,NN]
                                    = dom(m-halo+1:m,n-halo+1:n) ! to North-East
 V(m+1:m+halo,1-halo:0)[WW,NN]
                                    = dom(1:halo,n-halo+1:n)
                                                                   1
                                                                     to North-West
 V(1-halo:0,n+1:n+halo)[EE,SS]
                                    = dom(m-halo+1:m,1:halo)
                                                                   1
                                                                     to South-East
 V(m+1:m+halo,n+1:n+halo)[WW,SS]
                                    = dom(1:halo,1:halo)
                                                                   ! to South-West
 sync all
1
! Now run a stencil filter over the computational region (the region unaffected by halo values)
!
 do j=1,n
   do i=1,m
     sum = 0.
     do l=-halo, halo
       do k=-halo,halo
          sum = sum + stencil(k,l)*V(i+k,j+l)
        enddo
      enddo
      dom(i,j) = sum
    enddo
 enddo
```



Example code: CAF Put

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Example code: CAF Put

	:	
	V(1:m,1:n)	= dom(1:m,1:n)
	V(1-halo:0, 1:n)[EE,myQ]	<pre>= dom(m-halo+1:m,1:n)</pre>
	V(m+1:m+halo,n+1:n+halo)[WW,SS]	<pre>= dom(1:halo,1:halo)</pre>
	<pre>NO GLOBAL SYNCHRONIZATION HERE Perform filter over exclusive reg do j=1+halo,n-halo do i=1+halo,m-halo sum = 0. do l=-halo,halo do k=-halo,halo sum = sum + stencil(k,l)* enddo enddo dom(i,j) = sum enddo enddo</pre>	-
!	<pre>Pair-wise handshake synchronizati do mode=0,1 if (mod(myP,2) == mode) then sync images((myQ-1)*p+WW)</pre>	
1	<pre>do j=1+halo,n-halo do i=1,halo Apply filter dom(i,j) = sum enddo enddo else sync images((myQ-1)*p+EE) do j=1+halo,n-halo do i=m-halo+1,m :</pre>	! East

- ! internal region
- ! to East
- ! to South-West





Stencil 2D Results on XT5, XE6, X2; Halo = 1

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Using a fixed size virtual PE topology, vary the size of the local square

 XT5: CAF puts/gets implemented through message-passing library



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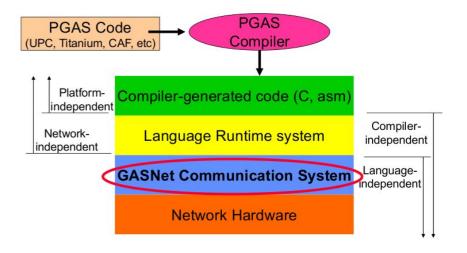
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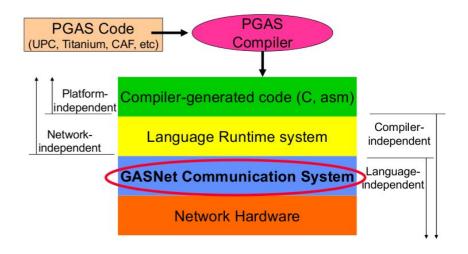


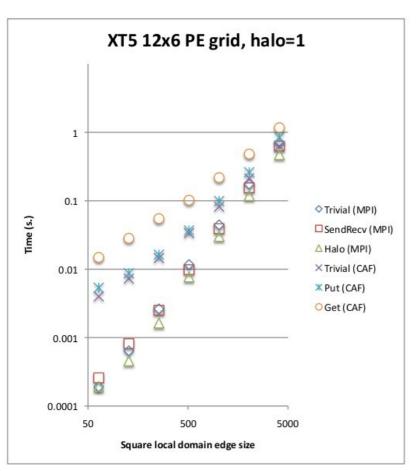




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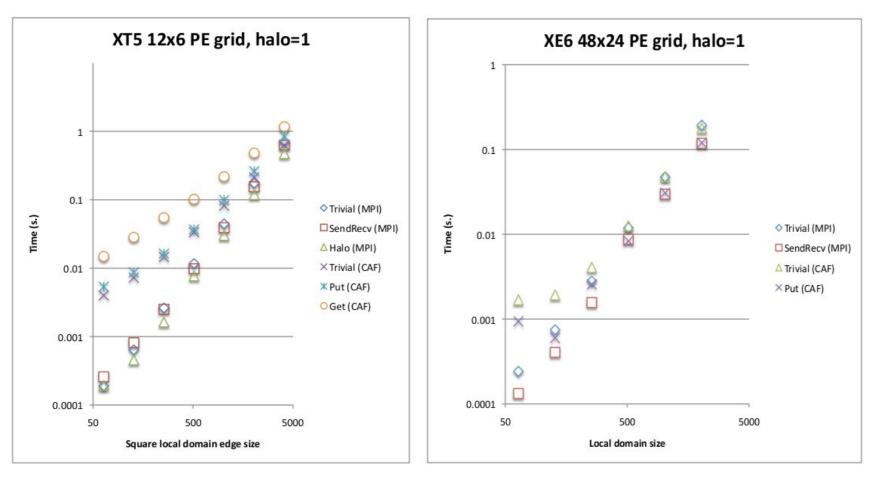


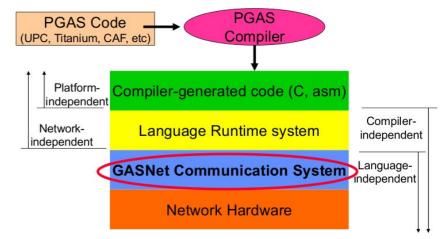




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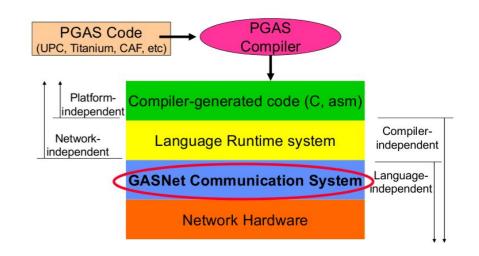


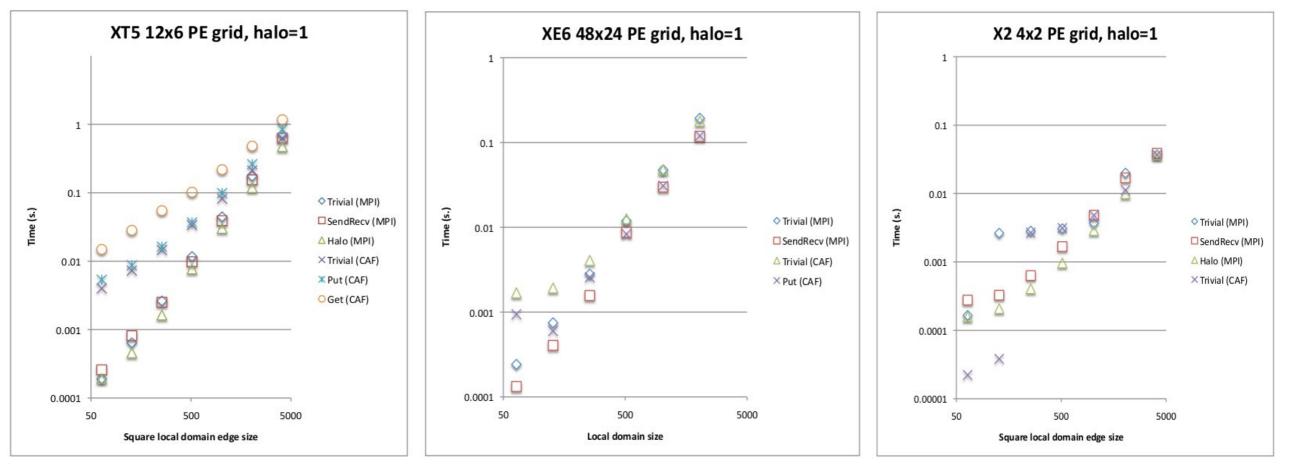




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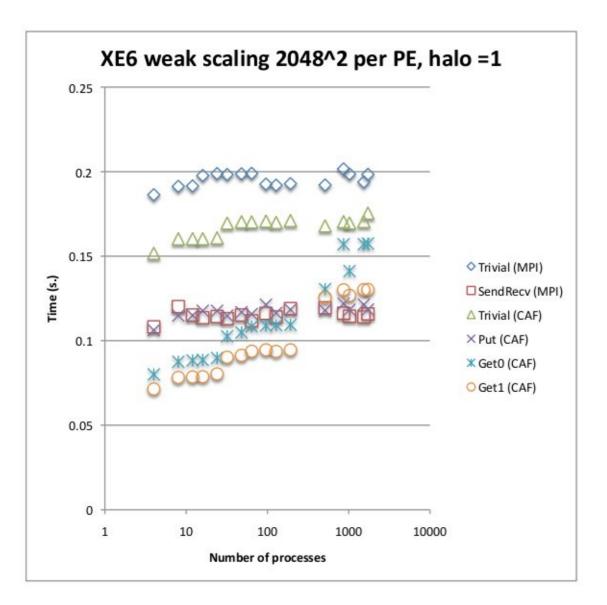
Stencil 2D Weak Scaling on XE6

Fixed local dimension, vary the PE virtual topology (take the optimal configuration)



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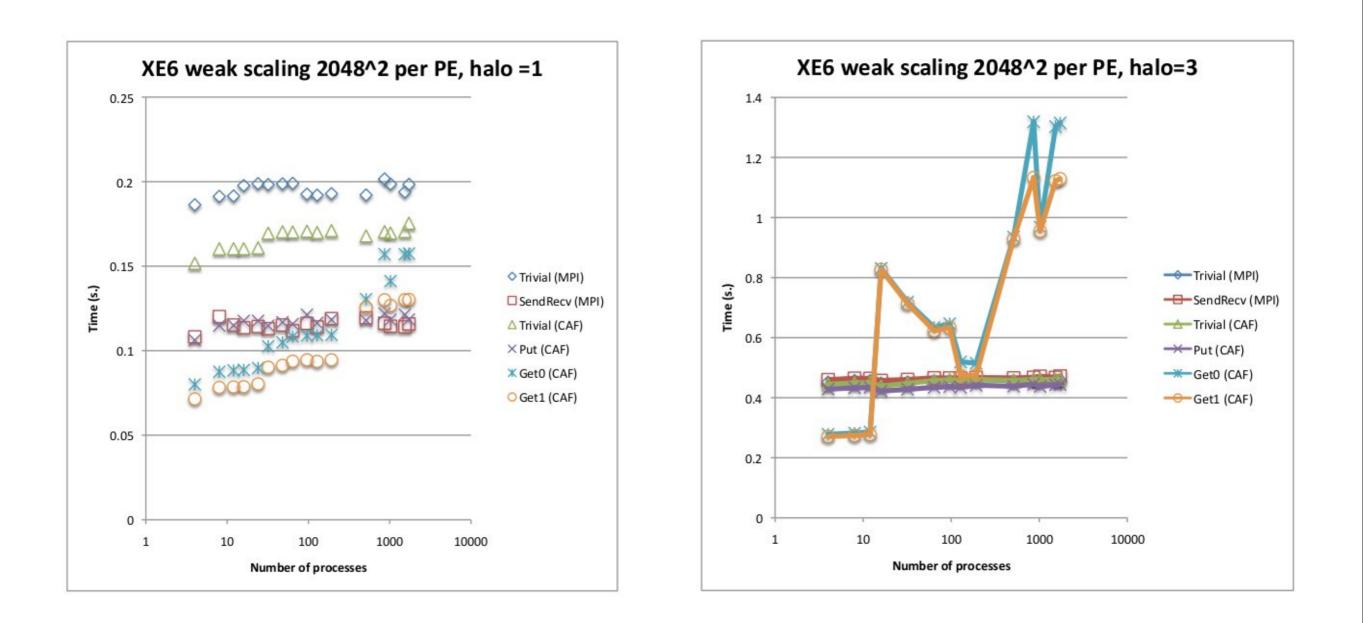
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Problem 2: Exact Diagonalization

$$H = J \sum S_i^z S_j^z + \Gamma \sum S_i^x$$

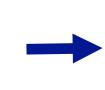


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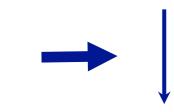


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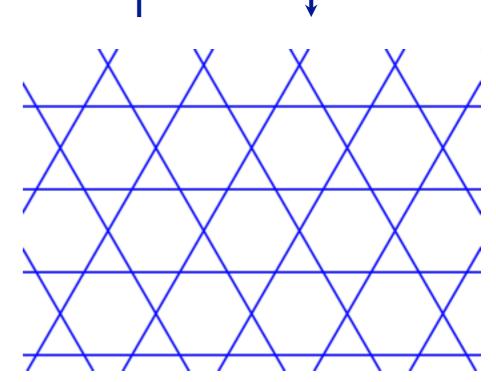
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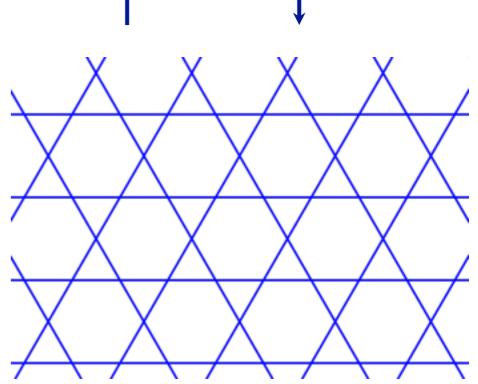
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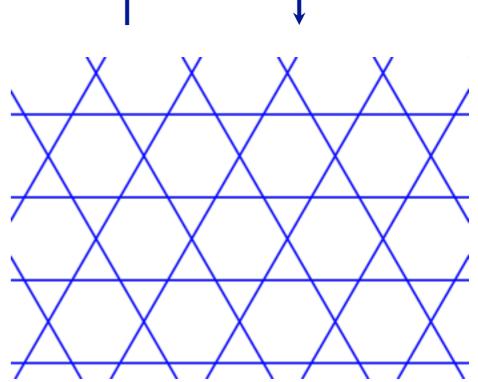
Algorithm 1 Lanczos iteration

1: $v_1 \leftarrow random$ vector with norm 1 2: $v_0 \leftarrow 0$ 3: $\beta_1 \leftarrow 0$ 4: for j = 1, ..., r do 5: $w_j \leftarrow Hv_j - \beta_j v_{j-1}$ 6: $\alpha_j \leftarrow (w_j, v_j)$ 7: $\beta_{j+1} \leftarrow ||w_j||$ 8: $v_{j+1} \leftarrow w_j / \beta_{j+1}$ 9: end for



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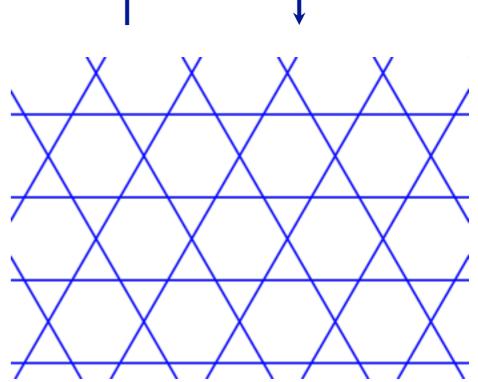
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4: for $j = 1,, r$ do			•.	
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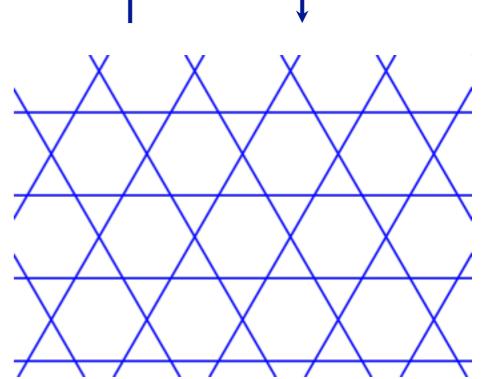
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Problem 2: Exact Diagonalization

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Any lattice with n sites, 2ⁿ states



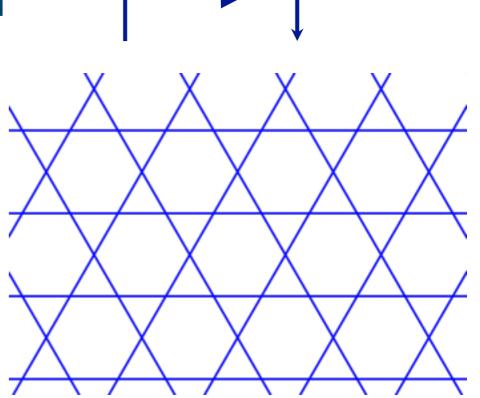
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- Any lattice with n sites, 2ⁿ states
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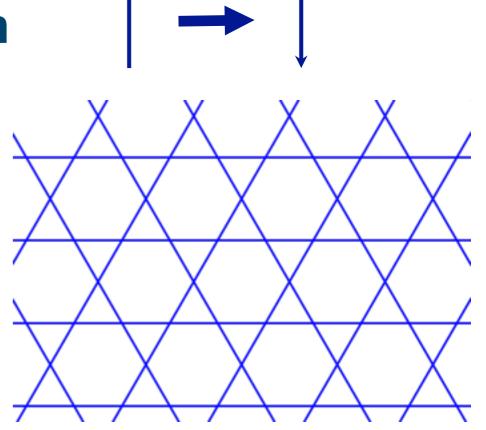


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- Any lattice with n sites, 2ⁿ states
- Lanczos eigensolver
- Large, sparse symmetric mat-vec

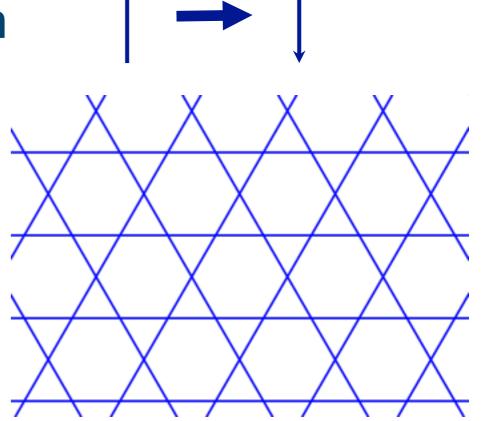


1			
α_1	β_2		
		۰.	
ρ_2	α_2	•	
	۰.	۰.	β_r
		Br.	α_r
L		191	
	$\begin{bmatrix} \alpha_1 \\ \beta_2 \end{bmatrix}$	$\begin{bmatrix} \alpha_1 & \beta_2 \\ \beta_2 & \alpha_2 \end{bmatrix}$	$\begin{bmatrix} \alpha_1 & \beta_2 \\ \beta_2 & \alpha_2 & \ddots \\ & \ddots & \ddots \\ & & & \beta_r \end{bmatrix}$



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- Large, sparse symmetric mat-vec
- Operator has integer operations

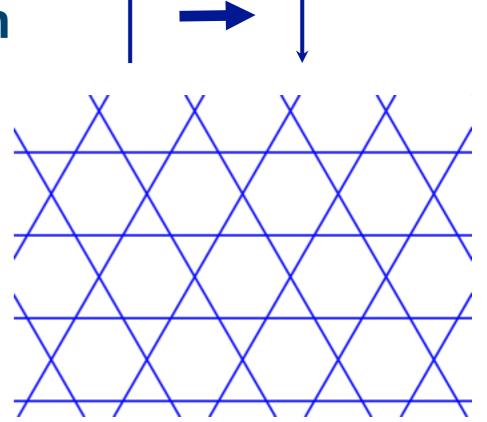


1: $v_1 \leftarrow$ random vector with no	orm 1
2: $v_0 \leftarrow 0$	
1: $v_1 \leftarrow \text{random vector with noise}$ 2: $v_0 \leftarrow 0$ 3: $\beta_1 \leftarrow 0$ 4: for $j = 1, \dots, r$ do 5: $w_j \leftarrow Hv_j - \beta_j v_{j-1}$ T_H 6: $\alpha_j \leftarrow (w_j, v_j)$ 7: $\beta_{j+1} \leftarrow w_j $ 8: $v_{j+1} \leftarrow w_j / \beta_{j+1}$	$\begin{bmatrix} \alpha_1 & \beta_2 \end{bmatrix}$
4: for $j = 1,, r$ do	
5: $w_j \leftarrow Hv_j - \beta_j v_{j-1} T_F$	$q = \begin{bmatrix} \beta_2 & \alpha_2 & \ddots & \\ & & & & & \\ & & & & & & \\ & & & &$
6: $\alpha_j \leftarrow (w_j, v_j)$	· · · · · β.
7: $\beta_{j+1} \leftarrow \ w_j\ $	Br Or
8: $v_{j+1} \leftarrow w_j / \beta_{j+1}$	$L \qquad p_r \alpha_r$
9: end for	



$$H = J \sum S_i^z S_j^z + \Gamma \sum S_i^x$$

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- Very irregular sparsity, but

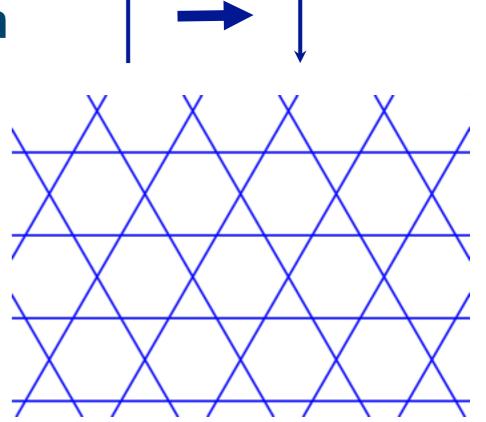


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4: for $j = 1,, r$ do			۰.	
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6: $\alpha_j \leftarrow (w_j, v_j)$		۰.	۰.	β_r
7: $\beta_{j+1} \leftarrow \ w_j\ $			ßm	0.
8: $v_{j+1} \leftarrow w_j / \beta_{j+1}$	L		ρr	α_{P}



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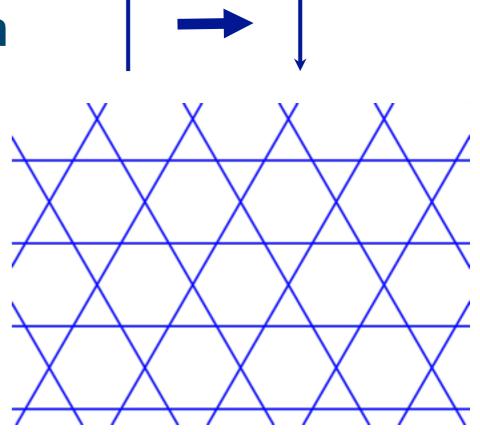


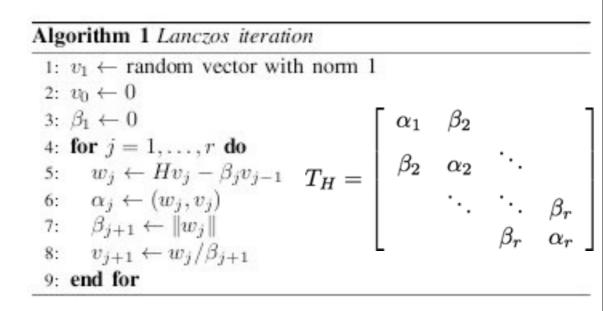
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- Very irregular sparsity, but
- Limited number of process neighbors (new to this work)
- Symmetries considered in some models: smaller complexity at cost of more communication









Benchmark code: simplest "SPIN" model

Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich



Benchmark code: simplest "SPIN" model

Loop for MAX_ITER

Reduction B (MPI_Reduce) L3 (local work, normalize v1) Loop over rounds of msgs MSG_NB (MPI_lsend,upc_memput(_nbi)) L4 (work on local matrix, only 1st iteration) SYNC (no-op, upc_fence) L7 (manage msg reception and do remote work) L8 (local work, A norm) Reduction A (MPI_Reduce) L9 (local work, B norm)

Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich



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- L3: Initialize array
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Benchmark code: simplest "SPIN" model

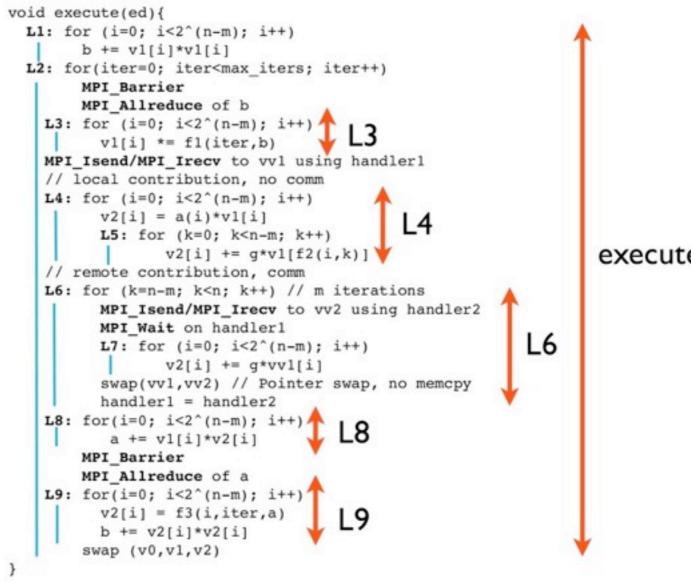
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Code structure



SPIN single core/socket/node comparisons

- Loop-based OMP directives: performance worse than MPI-only
- Task-based OpenMP/MPI implementation by Fourestey/Stringfellow

SPIN single core/socket/node comparisons

- Loop-based OMP directives: performance worse than MPI-only
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System name	Rivera	Castor	Sandy
Processor	AMD 6274	Intel E5-2680	Intel X5650
Nickname	Interlagos	Westmere	Sandybridge
Cores/Socket	16	6	8
Sockets/Node	2	2	2
Hyperthreading	no	unenabled	yes (2)
Compiler	Open64	Intel	Intel
Core time (s.)	754 (1T)	280 (1T)	227 (1T)
Socket time (s.)	74 (15T)	51 (6T)	29(16T)
Node time (s.)	38 (31T)	26 (12T)	15 (32T)

Multi-buffering concept

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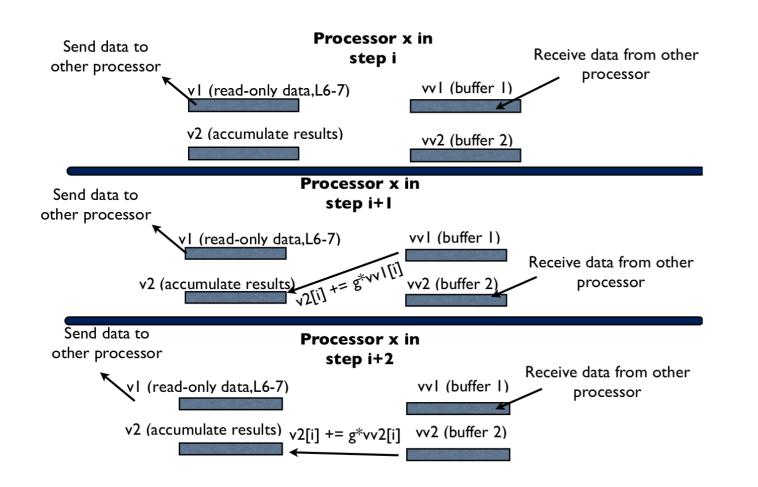
Multi-buffering concept

Double buffering



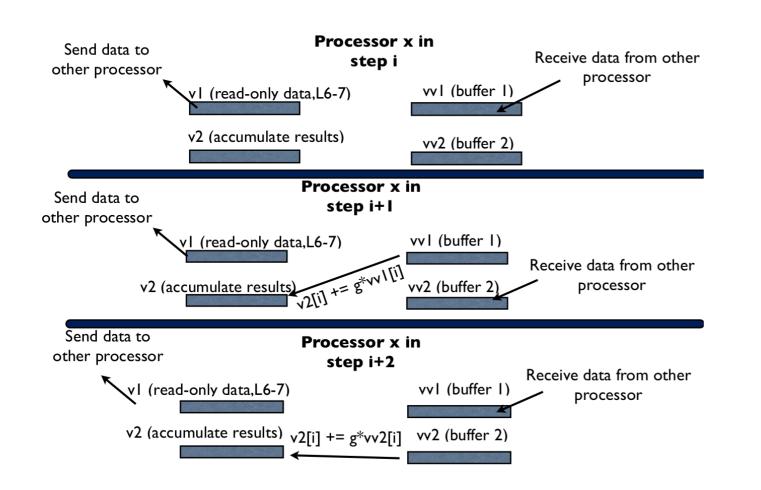
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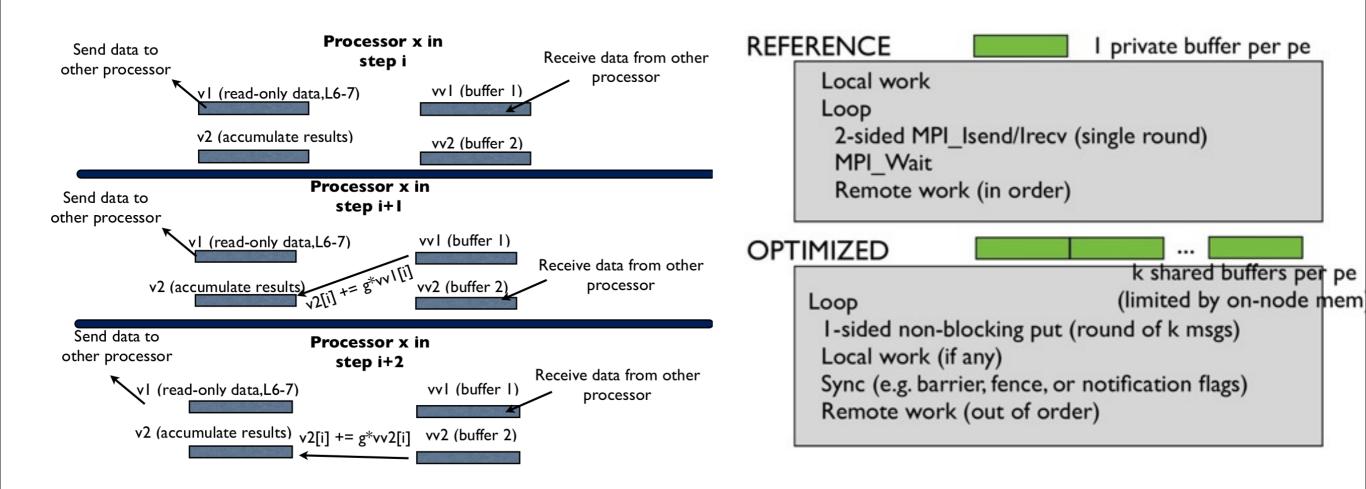


Multi-buffering

Multi-buffering concept

Double buffering

Multi-buffering



Sequential Implementation



Sequential Implementation

```
struct ed s { ...
        double *swap;
                                  /* for swapping vectors */
};
for (iter = 0; iter < ed->max iter; ++iter) {
                /* matrix vector multiplication */
                for (s = 0; s < ed -> nlstates; ++s) 
                        /* diagonal part */
                        ed - v2[s] = diag(s, ed - n, ed - j) * ed - v1[s];
                        /* offdiagonal part */
                        for (k = 0; k < ed ->n; ++k) {
                                s1 = flip state(s, k);
                                ed \rightarrow v2[s] += ed \rightarrow gamma * ed \rightarrow v1[s1];
                        }
                }
                /* Calculate alpha */
                /* Calculate beta */
        }
```

}





UPC "Elegant" Implementation

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UPC "Elegant" Implementation

```
struct ed s { ...
         shared double *v0, *v1, *v2; /* vectors */
         shared double *swap;
                                                 /* for swapping vectors */
};
for (iter = 0; iter < ed->max iter; ++iter) {
                  upc barrier(0);
                  /* matrix vector multiplication */
                  upc forall (s = 0; s < ed->nlstates; ++s; &(ed->v1[s]) ) {
                            /* diagonal part */
                            ed \rightarrow v2[s] = diag(s, ed \rightarrow n, ed \rightarrow j) * ed \rightarrow v1[s];
                            /* offdiagonal part */
                            for (k = 0; k < ed ->n; ++k) {
                                     s1 = flip state(s, k);
                                     ed \rightarrow v2[s] += ed \rightarrow gamma * ed \rightarrow v1[s1];
                            }
                   }
                   /* Calculate alpha */
                   /* Calculate beta */
         }
```

}

Inelegant UPC versions

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Inelegant UPC versions

Inelegant 1

```
shared[NBLOCK] double vtmp[THREADS*NBLOCK];

for (i = 0; i < NBLOCK; ++i) vtmp[i+MYTHREAD*NBLOCK] = ed->v1[i];
upc_barrier(1);
for (i = 0; i < NBLOCK; ++i) ed->vv1[i] = vtmp[i+(ed->from_nbs[0]*NBLOCK)];

upc_barrier(2);
```

Inelegant 2

```
shared[NBLOCK] double vtmp[THREADS*NBLOCK];
  :
upc_memput( &vtmp[MYTHREAD*NBLOCK], ed->v1, NBLOCK*sizeof(double) );
upc_barrier(1);
upc_memget( ed->vv1, &vtmp[ed->from_nbs[0]*NBLOCK], NBLOCK*sizeof(double) );
  :
upc_barrier(2);
```





UPC Inelegant3: use double buffers and upc_put

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UPC Inelegant3: use double buffers and upc_put

```
shared[NBLOCK] double vtmp1[THREADS*NBLOCK];
shared[NBLOCK] double vtmp2[THREADS*NBLOCK];
:
upc memput( &vtmp1[ed->to nbs[0]*NBLOCK], ed->v1, NBLOCK*sizeof(double) );
upc barrier(1);
if ( mode == 0 ) {
  upc_memput( &vtmp2[ed->to_nbs[neighb]*NBLOCK], ed->v1, NBLOCK*sizeof(double) );
 } else {
  upc memput( &vtmp1[ed->to nbs[neighb]*NBLOCK], ed->v1, NBLOCK*sizeof(double) );
 }
if ( mode == 0 ) {
  for (i = 0; i < ed->nlstates; ++i) { ed->v2[i] += ed->gamma * vtmp1[i+MYTHREAD*NBLOCK]; }
  mode = 1;
 } else {
  for (i = 0; i < ed->nlstates; ++i) { ed->v2[i] += ed->gamma * vtmp2[i+MYTHREAD*NBLOCK]; }
  mode = 0;
 }
upc barrier(2);
```





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MPI-2: One-sided PUT





MPI-2: One-sided PUT

MPI_Put(ed->v1, ed->nlstates, MPI_DOUBLE, ed->to_nbs[0], 0, ed->nlstates, MPI_DOUBLE, win1); MPI_Win_fence(0, win1);

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MPI-2: One-sided PUT

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SHMEM: non-blocking PUT





MPI-2: One-sided PUT

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SHMEM: non-blocking PUT

```
vtmp1 = (double *) shmalloc(ed->nlstates*sizeof(double));
   :
   shmem_barrier_all();
   shmem_double_put_nb(vtmp1, ed->v1, ed->nlstates, ed->from_nbs[neighb], NULL);
```





MPI-2: One-sided PUT

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SHMEM "fast": non-blocking PUT, local wait only





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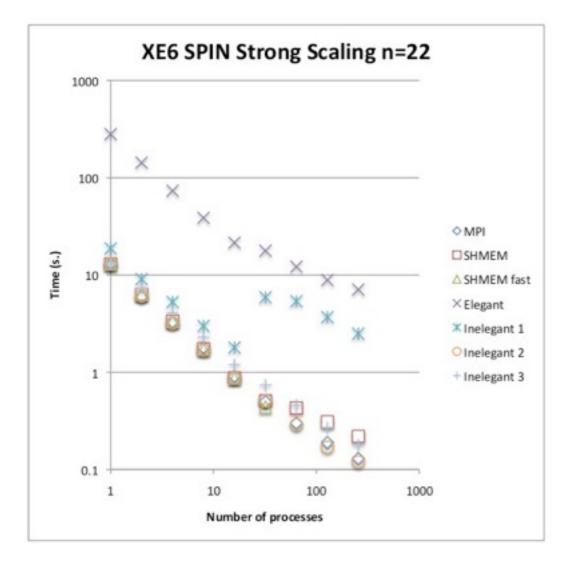
SPIN strong scaling: Cray XE6, n=22,24; 10 iter.

HP2C/Cray//CSCS Workshop





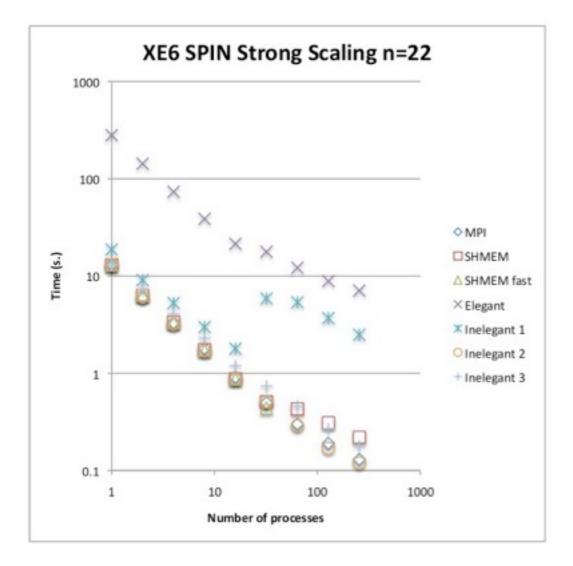
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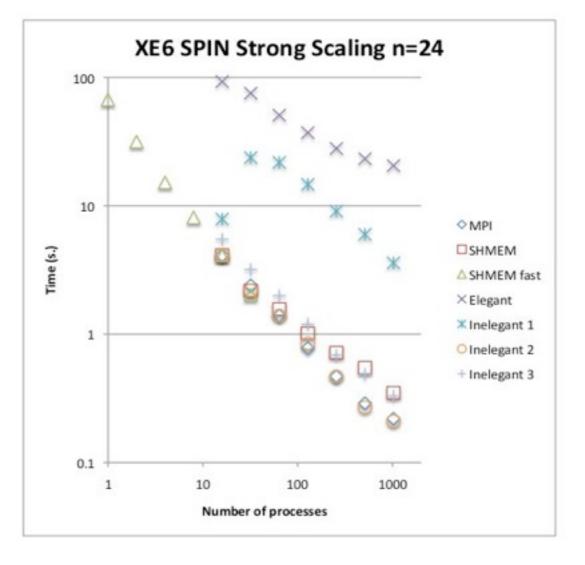






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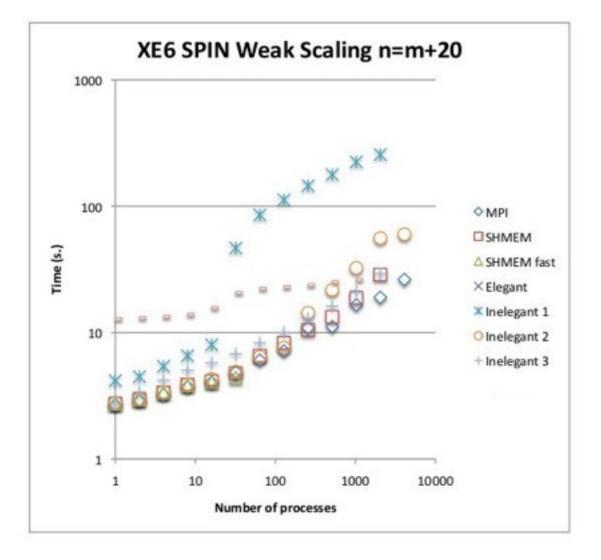


SPIN weak scaling: Cray XE6/Gemini, 10 iterations





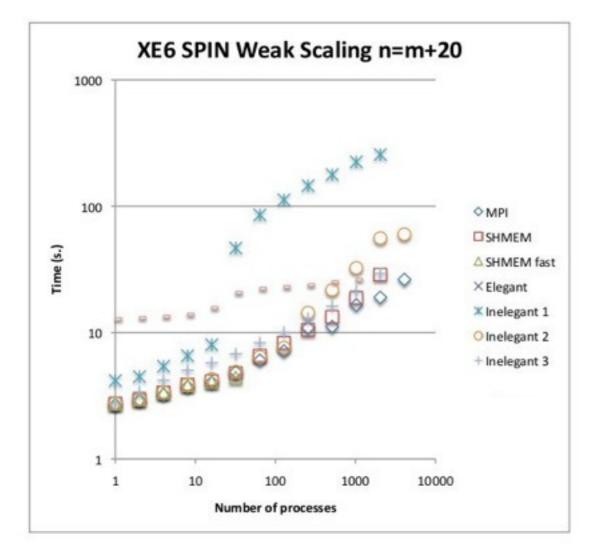
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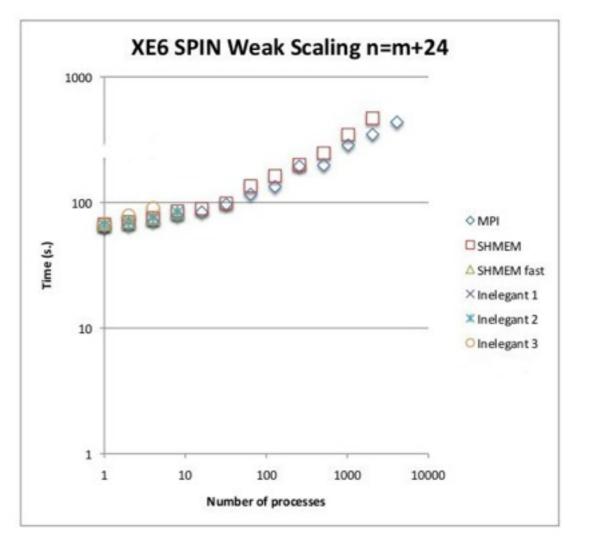






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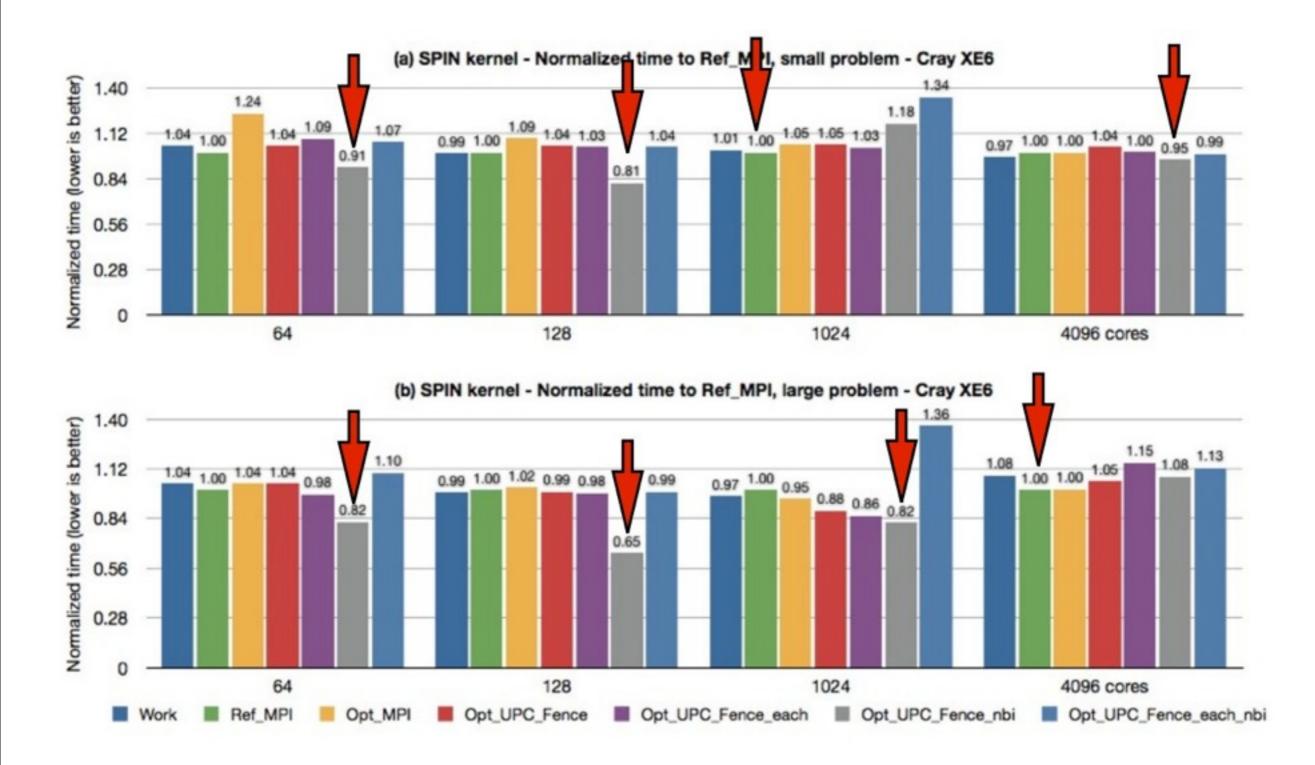
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Optimized SPIN normed performance: Cray XE6

Optimized SPIN normed performance: Cray XE6





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Take-home messages

PGAS languages can express communication elegantly





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- Inelegant PGAS implementations can outperform MPI
 - On platforms where PGAS is implemented close to the hardware, e.g., Cray XE6, X2
 - Where communication is explicitly formulated as PUTs or GETs, inherently defeating the purpose of the PGAS language





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 - Where communication is explicitly formulated as PUTs or GETs, inherently defeating the purpose of the PGAS language
- PGAS is worthwhile to keep in mind, but
- Currently the investment of changing paradigms does not seem worthwhile

Thank you for your attention! wsawyer@cscs.ch

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